Date: 18–19 March 2026
Time: 9:45 AM onwards

# Report on Two-Days Symposium

# on

# Semiconductor Technologies

The Two-Days Symposium on Semiconductor Technologies (SSIP) was organized by the Department of Electronics & Communication Engineering, G H Patel College of Engineering & Technology (GCET), CVM University, Vallabh Vidyanagar, in association with eInfochips (An Arrow Company), Ahmedabad, SSIP Cell GCET and ISTE. The symposium was conducted on 18–19 March 2026, starting from 9:45 AM onwards, at the K S Patel Auditorium, GCET. The event witnessed active participation from undergraduate students of Electronics & Communication Engineering, along with faculty members, making it a highly interactive and knowledge-enriching program. The symposium provided a platform for students to gain insights into recent advancements in semiconductor technologies and interact with industry experts.

## Objective of the Event

The primary objective of the symposium was to provide students with exposure to recent advancements in semiconductor technologies and to bridge the gap between academic learning and industry practices. The event aimed to enhance students' understanding of VLSI design flow, verification techniques, and emerging career opportunities in the semiconductor domain.

## Resource Persons / Experts

The two-day symposium comprised expert sessions focusing on key areas of semiconductor technology and VLSI design.

- **Session 1: Semiconductor Industry & Career Opportunities (Mr. Pinal Patel)**
  Provided an overview of the global semiconductor ecosystem, current industry trends, and various career paths. Emphasis was given to required technical skills and industry expectations.
- **Session 2: RTL Design & Hardware Implementation (Mr. Vimal Mer)**
  Covered fundamentals of RTL design, digital design flow, and hardware implementation concepts. Practical insights into coding practices and design methodologies were discussed.

- **Session 3: SystemVerilog for Functional Verification (Mr. Ashish Christian)**
  Focused on verification methodologies using SystemVerilog, importance of testbenches, and ensuring functional correctness of digital designs.
- **Session 4: Design for Test (DFT) Techniques (Ms. Illa Vaghela)**
  Explained various DFT techniques such as scan chains and fault detection methods to improve chip reliability and testability.
- **Session 5: Physical Design for Complex SoC (Dr. Dipesh Panchal)**
  Discussed physical design flow including placement, routing, timing closure, and challenges in modern SoC design.

## Contents Covered

The sessions covered the following key topics:

- Semiconductor Industry Trends and Career Opportunities
- RTL Design and Hardware Implementation
- System Verilog for Functional Verification
- Design for Test (DFT) Techniques
- Physical Design for Complex System-on-Chip (SoC)

## Outcomes of the Event

The symposium resulted in the following outcomes:

- Students gained insights into real-world semiconductor industry practices.
- Enhanced understanding of VLSI design flow including RTL, verification, and physical design.
- Awareness of career opportunities in semiconductor and electronics industries.
- Exposure to industry expectations and required skill sets.
- Improved motivation among students to pursue careers in VLSI and embedded systems.
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## Conclusion

The Two-Days Symposium on Semiconductor Technologies was successfully conducted with active participation from students and faculty members. The sessions delivered by industry experts were highly informative and aligned with current industry requirements. The event significantly contributed to **academic enrichment and professional development of students**, fulfilling the objectives of outcome-based education as required by NBA.

# PHOTOGRAPHS:


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